SYSTEM FOR ERROR CORRECTION CODING AND DECODING

Background of the Invention

[0001] Error detection and correction codes are widely used in communication and storage systems to provide reliable information transmission and recovery. Communication systems can be susceptible to errors in the form of signal degradation which results in distortion or noise in transmitted signals. Signal degradation can also result in a loss of transmitted information. Systems which are susceptible to signal degradation or information loss include wireless or mobile communications systems such as cellular telephone, microwave systems, satellite communications systems, digital television and high speed communications systems such as those that utilize an xDSL communication standard.

[0002] Memory storage systems can also be susceptible to errors which result in a loss of stored information. The errors can occur from reliability degradation which causes physical failures within individual memory storage devices. Failure mechanisms which can result from reliability degradation include time dependent dielectric breakdown and electromigration, both common in complementary metal oxide semiconductor (CMOS) integrated circuits.

[0003] A number of error correction techniques exist which can be used to detect and correct errors in information, or counteract the effects of signal degradation. The error correction techniques typically use additional amounts of information which can be added to the original stored or transmitted information. The additional information is generated from an error correction code, and is used to check the validity of the original information. The most common types of error correction codes are convolutional (tree) codes and block codes. With these codes, the information is separated into blocks, and each block is encoded into a larger block of data.

[0004] Error correction codes can have varying abilities to detect and correct errors. Stronger error detection and correction codes, for example, will allow information to be transmitted and received with lower error rates. These

stronger error correction codes usually require more powerful processors or controllers to execute the codes and transmit or store the additional error correction code bits.

[0005] The strength of the error correction code is typically chosen for a particular system or application. Once a particular error correction code is chosen for the system or application, the associated execution time or latency time is fixed. In other words, if a higher degree of reliability is required, and high latency error correction routines are used, the system or application will always have the same throughput, even if the reliability requirements are later reduced.

Summary of the Invention

[0006] Embodiments of the present invention provide a system and method for error correction coding and decoding of information. In one embodiment, first and second encoders are each configured to encode the information, wherein the second encoder has a higher capability than the first encoder. The first and second decoders are configured to recover the information, wherein the second decoder recovers the information encoded by the second encoder only if the first decoder cannot recover the information.

Brief Description of the Drawings

[0007] Embodiments of the invention are better understood with reference to the following drawings. The elements of the drawings are not necessarily to scale relative to each other. Like reference numerals designate corresponding similar parts.

[0008] Figure 1 is a diagram illustrating an exemplary embodiment of a system for error correction coding and decoding.

[0009] Figure 2 is a diagram illustrating an exemplary embodiment of a logical data structure.

[0010] Figure 3 is a diagram illustrating a first embodiment of first and second encoders.

[0011] Figure 4 is a diagram illustrating a first embodiment of a codeword.

[0012] Figure 5 is a diagram illustrating a second embodiment of first and second encoders.

[0013] Figure 6 is a diagram illustrating a second embodiment of a codeword.

[0014] Figure 7 is a diagram illustrating an exemplary embodiment of first and second decoders.

Detailed Description

[0015] Figure 1 is a diagram illustrating an exemplary embodiment of a system for error correction coding and decoding. The system 10 includes an encoding system 12/112 and a decoding system illustrated at 24. The encoding system 12/112 includes a first encoder 14/114 and a second encoder 16/116. An information block or block of digital data is provided at input 18. The information block is encoded to produce a codeword at 20 by combining the information, first parity symbols generated by first encoder 14/114 and second parity symbols generated by second encoder 16/116. The format of the information block and codeword is described in more detail in Figure 2. In the exemplary embodiment, the second encoder 16/116 has a higher capability to detect and correct errors than the first encoder 14/114. The second encoder generates a number of second parity symbols which is greater than the number of the first parity symbols. The increased number of second parity symbols allows a greater number of errors or erasures to be detected and corrected. In a first exemplary embodiment, the information block is encoded by combining the information, the first parity symbols generated when the first encoder 14 encodes the information, and the second parity symbols generated when the second encoder 16 encodes the information. In a second exemplary embodiment, the second encoder encodes both the information and the first parity symbols.

[0016] In the exemplary embodiment, the decoder system 24 includes a first decoder 26 and a second decoder 28. Decoder system 24 decodes the codeword, which is provided at input 22, and provides the information block at output 30. In the exemplary embodiment, the information block at output 30 is equivalent

to the information block at 18. In other embodiments, substantial portions of the information block at 18 and 30 are equivalent.

[0017] In the exemplary embodiment, first decoder 26 is configured to recover the information block by detecting and correcting errors and erasures using the first parity symbols generated when first encoder 14/114 encodes the information. The first decoder 26 provides an indication if the information block cannot be recovered from the codeword provided at input 22. In other embodiments, any suitable approach can be used to indicate that the information block cannot be recovered. In the exemplary embodiment, second decoder 28 is configured to recover the information using the second parity symbols generated when second encoder 16/116 encodes the information. The second decoder recovers the information block only if the first decoder 26 cannot detect and correct one or more errors and erasures, or if the first decoder 26 provides the indication. In various embodiments, the indication is a flag or signal which indicates that the information block was not recovered by the first decoder 26.

[0018] In the exemplary embodiment, second decoder 28 is configured to recover the information by using second parity symbols. In a first exemplary embodiment, the second parity symbols are generated when second encoder 16 encodes the information block (see also, Figure 3). In a second exemplary embodiment, the second parity symbols are generated when the second encoder 116 encodes both the information block and the first parity symbols generated when the first encoder 114 encodes the information block (see also, Figure 5).

[0019] In various embodiments, any suitable error correction code can be used. In one embodiment, the first and second encoders and the first and second decoders use a Reed-Solomon code. Reed-Solomon codes are block-based error correcting codes which are used for a wide range of communication and storage applications. In another embodiment, the first and second encoders and first and second decoders use a linear block code. In one embodiment, the linear block code is a cyclic redundancy check code. In another embodiment, first encoder and first decoder use a cyclic redundancy check (CRC) with error detection capability and with no correction capability. The second encoder and second

decoder use a Reed-Solomon code with error correction capability. In other embodiments, the first and second encoders and first and second decoders use other suitable error correction and detection codes, such as a convolutional code, first-correcting code, a hamming code, etc.

[0020] In one embodiment, the first encoder 14/114 and the second encoder 16/116 use the Reed Solomon code to encode the information block. The Reed-Solomon code is specified using (n,k) with s-bit symbols. First encoder 14/114 or second encoder 16/116 take k data symbols of s bits each and add parity symbols to make an n symbol codeword. There are n-k parity symbols of s bits each in the codeword. First decoder 26 or second decoder 28 decode the codeword and can correct up to t symbols that contain errors in the codeword, where 2t = n-k. Because the second encoder 16/116 generates the number of second parity symbols which is greater than the number of first parity symbols generated by the first encoder 14/114, the second decoder 28 can detect and correct a greater number of errors or erasures than the first decoder 26.

[0021] In one exemplary embodiment using the Reed-Solomon code, first encoder 14/114 accepts one byte (or symbol) at a time until it has processed a 128-btye information block. First encoder 14/114 accepts an information block at input 18 in the byte format, and takes one or more bytes of latency time to process the information. In the exemplary embodiment, the codeword at 20 is also in a byte format. Second encoder 16/116 also processes the information in a byte format, and has a latency time of one or more times to process the information. In one embodiment, first encoder 14/114 and first decoder 26 have a stronger error detection capability and a weaker error correction capability than second encoder 16/116 and second decoder 28.

[0022] In various embodiments, encoding data using first encoder 14/114 and second encoder 16/116 is a relatively simple operation, and as such, the encoding process can be easily synthesized using electrical circuits or transistor gates. The performance penalty incurred for encoding the information block using first encoder 14/114 versus second encoder 16/116 is minimal, and

generating the additional parity symbols in the second parity symbols has a minimal impact on the byte time latency necessary to process the codeword.

[0023] In the exemplary embodiment, first encoder 14/114 generates a number of first parity symbols or bits which are used by first decoder 26 to decode the codeword at input 22 into the information block at output 30. First decoder 26 has a latency time to process the codeword into the information block at output 30 which is less than the latency time of second decoder 28. If the error detection and correction capability of first decoder 26 is insufficient to correct errors detected in the codeword, the second decoder 28 decodes the codeword into the information block at 30. Second decoder 28 has a higher latency time than first decoder 26, but only decodes the codeword at 22 into the information block at 30 when first decoder 26 cannot correct the errors or erasures, or when first decoder 26 provides an indication that the errors or erasures cannot be corrected. In the exemplary embodiment, first decoder 26 and second decoder 28 process the codeword which includes the information block and the parity symbols, and detects and corrects any erasures which exist. With the Reed-Solomon system, the latency time of the first decoder 26 or the second decoder 28 can be significantly greater than the latency time of the first encoder 14/114 or the second encoder 16/116. In one exemplary embodiment, first decoder 26 and second decoder 28 require significantly more electrical circuits or transistor gates to synthesize than first encoder 14/114 and second encoder 16/116.

[0024] Figure 2 is a diagram illustrating an exemplary embodiment of a logical data structure. In one embodiment, original information 42 is received in predetermined units such as a sector comprising 512 bytes. In the exemplary embodiment, error correction coding is performed to produce a block of encoded data 44, in this case an encoded sector. The encoded sector 44 comprises a plurality of symbols 48, which can be a single bit (e.g. a BCH code with single bit symbols) or can comprise multiple bits (e.g. a Reed-Solomon code using multi-bit symbols). In one Reed-Solomon encoding scheme, each symbol 48 conveniently comprises eight bits. As shown in Figure 2, the encoded sector 44 comprises four codewords 46, each comprising a number of symbols, such as

144 to 160 symbols. In one embodiment, the eight bits corresponding to each symbol are conveniently stored in eight storage cells of a memory storage device. In the exemplary embodiment, a failure which affects any of the eight storage cells can result in one or more of the bits being unreliable (i.e. the wrong value is read) or unreadable (i.e. no value can be obtained), thus giving a failed symbol.

[0025] In the exemplary embodiment, error correction decoding the encoded data 44 allows failed symbols 48 to be identified and corrected. The preferred Reed-Solomon scheme is an example of a linear error correcting code, which mathematically identifies and corrects completely up to a predetermined maximum number of failed symbols 48, depending upon the power of the code. For example, a [160,128,33] Reed-Solomon code producing codewords having 160 bit symbols corresponding to 128 original information bytes and a minimum distance of 33 symbols can locate and correct up to 16 symbol errors. Suitably, the ECC scheme employed is selected with a power sufficient to recover original information 42 from the encoded data 44.

[0026] Figure 3 is a diagram illustrating a first embodiment of first and second encoders 14 and 16. The encoding system is shown generally at 12. First encoder 14 and second encoder 16 are configured to encode the information. In the exemplary embodiment, the second encoder 16 has a higher capability than the first encoder 14. By "higher capability," it is meant that the second encoder 16 can correct a larger number of errors than first encoder 14. For example, first encoder 14 may utilize a Reed-Solomon code producing codewards of 132 eight-bit symbols corresponding to 128 original data bytes that can locate and correct up to two random errors in 132 bytes. Second encoder 16 may utilize a Reed-Solomon code having a high capability relative to first encoder 14, producing codewords of 160 eight-bit symbols corresponding to 128 original data bytes that can locate and correct up to 16 random errors in 160 bytes.

[0027] First encoder 14 and second encoder 16 each include as an input the information block at 18. First encoder 14 has an output 50 which is coupled to an input of a time division multiplexer 54. Second encoder 16 has an output 52

which is coupled to an input of time division multiplexer 54. Time division multiplexer 54 has a select input at 56 which selects between output 50 of first encoder 14 and output 52 of second encoder 16. The selected codeword at input 50 or input 52 is coupled to an output at 20. In the exemplary embodiment, any suitable means can be used to provide a control input at 56 to time division multiplexer 54 to select between input 50 and input 52. Time division multiplexer 54 is configured to combine the information block, the first parity symbols generated by first encoder 14 and the second parity symbols generated by second encoder 16 into the codeword. The codeword is illustrated in Figure 4.

[0028] In the exemplary embodiment, second encoder 16 has a higher capability than first encoder 14, and as such, second encoder 16 generates a number of the second parity symbols which is greater than a number of the first parity symbols generated by first encoder 14. In the exemplary embodiment, the block of information at 18 is fed simultaneously to first encoder 14 and second encoder 16. First encoder 14 encodes the information block at 18 into a codeword which includes the information block and first parity symbols. Second encoder 16 encodes the information block at 18 into a codeword at 52 which includes the information block and second parity symbols. Time division multiplexer 54 multiplexes the information block, the first parity symbols and the second parity symbols into the codeword which is provided at output 20.

[0029] Figure 4 is a diagram illustrating a first embodiment of a codeword. The codeword is illustrated generally at 60. The codeword includes the information block which is illustrated at 32, first parity symbols which are illustrated at 62 and second parity symbols which are illustrated at 64. Time division multiplexer 54 combines the information block, the first parity symbols and the second parity symbols into the single codeword format illustrated at 60. The information is encoded to produce a codeword by combining the information, first parity symbols generated when the first encoder encodes the information and the second parity symbols generated when the second encoder encodes the information.

[0030] In one embodiment, first encoder 14 is a first error correction coding (ECC) encoder circuit which is configured to generate first parity symbols. Second encoder 16 is a second ECC encoder circuit that is configured to generate second parity symbols. The number of the second parity symbols is greater than the number of the first parity symbols. The first parity symbols, the second parity symbols and the information block or data are combined into a codeword at 20.

[0031] Figure 5 is a diagram illustrating a second embodiment of first and second encoders. The encoding system is illustrated generally at 112. First encoder 114 and second encoder 116 are configured to encode the information block received at 18. Second encoder 116 has a higher capability than first encoder 114. In the exemplary embodiment, second encoder 116 generates a number of the second parity symbols which are greater than the number of first parity symbols generated by the first encoder 114.

[0032] In the exemplary embodiment, an information block is input at 18 to first encoder 114. First encoder 114 generates an output at 70 which includes the information block and first parity symbols appended to the information block. The output codeword from first encoder 114 at line 70 is fed into the second encoder 116. Second encoder 116 appends second parity symbols to the codeword received at 70, and outputs a codeword at 20 which includes both the first parity symbols and the second parity symbols. In the exemplary embodiment, the encoding system 112 encodes the information block and provides an output codeword at 20 which includes the information block, first parity symbols generated when first encoder 114 encodes the information, and second parity symbols generated when second encoder 116 encodes both the information block and the first parity symbols.

[0033] In one exemplary embodiment, first encoder 114 and second encoder 116 are error correction coding (ECC) circuits. First ECC encoder circuit 114 is configured to generate first parity symbols from the information block or data. Second ECC encoder circuit 116 is configured to generate second parity symbols from the output of first encoder 114 at 70. The second parity symbols are

generated from both the information block and the first parity symbols. The number of the second parity symbols is greater than the number of the first parity symbols. The first parity symbols, the second parity symbols and the information or data are combined into the codeword at output 20.

[0034] Figure 6 is a diagram illustrating a second embodiment of a codeword. The codeword is illustrated generally at 80. The codeword 80 includes the information block at 32, first parity symbols at 162 and second parity symbols at 164. The information block is provided at input 18 to first encoder 114. The output of first encoder 114 at 70 is illustrated as a second encoder information block and includes the information block at 32 and the first parity symbols at 162. The output of second encoder 116 at 20 includes the information block at 32, the first parity symbols at 162 and the second parity symbols at 164, which are appended into a single codeword 80.

[0035] Figure 7 is a diagram illustrating an exemplary embodiment of first and second decoders 26 and 28. The decoder system is illustrated generally at 24. In first and second exemplary embodiments, first decoder 26 is configured to recover the information block using first parity symbols generated when the first encoder 14/114 encodes the information block. In the first and second exemplary embodiments, first decoder 26 is configured to provide an indication if the information block cannot be recovered. In the first and second exemplary embodiments, the indication is an output flag provided at 90. In other embodiments, the indication can be provided by any suitable means. In the first exemplary embodiment, second decoder 28 is configured to recover the information block by using second parity symbols generated when the second encoder 16 encodes the information block. In the second exemplary embodiment, second decoder 28 is configured to recover the information block using second parity symbols generated when second encoder 116 encodes both the information block and the first parity symbols. In the first and second exemplary embodiments, the second decoder 28 recovers the information block only if the first decoder 26 provides the indication at 90.

[0036] In the exemplary embodiment, second decoder 28 includes a buffer 98, a processor system 102, wherein buffer 98 is coupled to processor system 102 via line 100. Buffer 98 is configured to store the information block and the second parity symbols. Processor system 102 is configured to recover the information block by using the second parity symbols only if the first decoder 26 provides the indication at 90. Processor system 102 includes an input at 104 which is configured to receive the indication provided at 90. In various embodiments, suitable control circuitry (not illustrated) has the output at 90 as an input and provides an output to the input at 104 to control processor system 102. The output of first decoder 26 at 92 and the output of second decoder 28 at 106 couple into a select circuit at 94. Select circuit 94 selects, via a control input provided at 96, either the codeword provided by first decoder 26 which is provided at 92, or the codeword provided by second decoder 28, which is provided at 106. Select circuit 94 outputs the selected information block at 30.

[0037] In the exemplary embodiment, first decoder 26 recovers the information using the first parity symbols to detect and correct any errors in the information block. Second decoder 28 recovers the information using the second parity symbols to detect and correct any errors in the information block.

[0038] In the exemplary embodiment, the codeword provided at 22 is an input to first decoder 26 and second decoder 28. The information portion of the codeword is provided to first decoder 26 along with the first parity symbols. First decoder 26 determines whether there are errors or erasures in the codeword using the first parity symbols. If there are no errors or erasures detected, first decoder 26 discards the first parity symbols and the second parity symbols from the codeword, and provides the information block at output 92. If there are errors in the codeword, first decoder 26 determines whether the errors or erasures can be corrected. If first decoder 26 can correct the errors or erasures in the codeword, the corrected information is provided at 92, and both the first parity symbols and the second parity symbols are discarded. If there are errors or erasures in the codeword which first decoder 26 cannot correct, first decoder 26 provides an indication at 90 to input 104 of processor system 102 to indicate

that first decoder 26 has encountered an unrecoverable error. In the exemplary embodiment, the codeword is stored in buffer 98. Processor 102 uses a suitable hardware or software algorithm along with the parity from second encoder 16/116 to correct the errors or erasures in the information. Once the processor system 102 completes the execution of the algorithm and corrects any errors or erasures in the information within the codeword, the processor discards the first parity symbols and the second parity symbols and outputs the information block at 106. Select circuit 94 selects either the information block provided at 92 from first decoder 26 or the information block provided at 106 from second decoder 28. Suitable control circuitry (not illustrated) provides a control input at 96 to make the selection. The selected information block is output at 30.

[0039] In an exemplary method of error correction coding of information, a number of first parity symbols are generated from the information block. The first parity symbols are generated by first encoder 14/114. Next, a number of second parity symbols are generated from the information block by second encoder 16/116. In the exemplary embodiment, the number of the second parity symbols is greater than the number of the first parity symbols. Next, the first parity symbols, the second parity symbols and the information are combined into an encoded data block.

[0040] In an exemplary method of decoding the information block, the information block is recovered from the codeword or encoded data block using the first parity symbols if the information block can be recovered using the first parity symbols. The information is recovered from the codeword or encoded data block using the second parity symbols only if the information cannot be recovered using the first parity symbols.

[0041] In the exemplary method, the information block is recovered from the codeword or encoded data block using the first parity symbols and includes detecting and correcting errors or erasures in the information block which can be detected or corrected using the first parity symbols. In the exemplary method, the information block is recovered from the codeword or encoded data block using the second parity symbols and includes detecting or correcting errors or

erasures in the information block which can be detected or corrected using the second parity symbols. In one embodiment, generating a number of the second parity symbols from the information block includes generating a number of the second parity symbols from both the first parity symbols and the information block. In this embodiment, recovering the information block from the codeword or encoded data block using the second parity symbols includes detecting or correcting errors in the first parity symbols and the information block using the second parity symbols.